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(54) POKER MACHINE

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(74) SW

(57) Claim

1. A random payment awarding apparatus for connection to a plurality of poker machines each adapted to produce an incrementing signal at each operation thereof, said apparatus comprising means to generate and store a random number within a selected range; counting means adapted to increment through the numbers in said range, each increment being effected on receipt of an incrementing signal from one of said poker machines; comparator means to compare said random number and the number held in said counting means; means to record the identity of the poker machine that emitted the last incrementing signal if said random number and the number held in said counting means are equal; and display means to display the number held in said counting means after each said increment and operable to display a prize award indication and the identity of the poker machine that emitted the last incrementing signal if said random number and the number held in said counting means are equal.

2. An apparatus as claimed in claim 1 wherein said .../2

random number is indicative of an amount of money to be payed to the player playing the machine which emitted the last incrementing signal.

3. An apparatus as claimed in claim 1 or claim 2 wherein each poker machine is electrically isolated from the random payment awarding apparatus.

FORM 10

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COMPLETE SPECIFICATION

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Complete Specification for the Invention entitled: "A RANDOM PAYMENT AWARDING APPARATUS".

The following statement is a full description of this invention, including the best method of performing it known to me/us:—
Complete of PG9210 and dated 8th February, 1985

SW16

The present invention relates to apparatus for use with poker machines and, in particular, to apparatus for awarding additional prizes to poker machine players.

Numerous methods have been devised to induce people to play poker machines. Commonly, these include schemes such as stipulating a time interval during which jackpots are increased, or awarding an additional prize to the first player to "pull" a predetermined combination on a poker machine. Whilst these methods are effective they present difficulties in administration and require additional staff to ensure smooth operation.

It is an object of the present invention to provide a random payment awarding apparatus which will overcome, or at least ameliorate the abovementioned disadvantages.

According to the present invention there is provided a random payment awarding apparatus for connection to a plurality of poker machines each adapted to produce an incrementing signal at each operation thereof, said apparatus comprising means to generate and store a random number within a predetermined range; counting means adapted to increment through the numbers in said range, each increment being effected on receipt of an incrementing signal from one of said poker machines; comparator means to compare said random number and the number held in said counting means; means for recording the identity of the poker machine which emitted the last incrementing signal if said random number and the number held in said counting means are equal; and display means

to display the number held in said counting means after each increment and operable to display a prize award indication and the identity of the poker machine which emitted the last incrementing signal if said random number and the number held in said counting means are equal.

Preferrably, the random number is indicative of an amount of money which is payed to the player playing the machine which emitted the last incrementing signal.

One embodiment of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a schematic block diagram of the circuitry of the random payment awarding apparatus;

Figure 2 is a circuit diagram of the processor shown schematically in Figure 1;

Figure 3 is a circuit diagram of interface 1 shown schematically in Figure 1; and

Figure 4 is a circuit diagram of interface 2 shown schematically in Figure 1.

Referring to Figure 1 the random payment awarding apparatus is first described in outline.

The apparatus comprises a processor 10 which forms means to generate and store a random number. The allowable values of the random number is determined by a table stored in programable read only memory (PROM) in the processor 10. The range and hence the maximum prize can only be altered by changing the table. The random

number is generated by a free running counter (not illustrated) within the processor 10 which "rolls over" at the maximum prize value. The counter is stopped by initial setting through input 12 to interface 11 which transmits a signal to processor 10, or by the first operation of one of the connected poker machines. The value of the random number is not revealed by the apparatus until a prize is awarded.

A pulse collecting interface 11 is connected with the processor 10 and in conjunction interface 11 and processor 10 form counting means adapted to increment through the selected range of random numbers. Each increment is effected on receipt by interface 11 of an incrementing signal from a poker machine (not shown) connected with the apparatus via inputs 13 or 14. Input 12 is provided for initial setting and resetting of the apparatus.

In operation, the inputs 13 and 14 are connected to the stroke meters of substantially conventional poker machines (not illustrated). Only two inputs are shown but in the circuits of Figures 2 and 3 provision is made for up to 24 inputs. On operation of one of the poker machines a signal is transmitted to interface 11 which increments a count number stored in processor 10 by a predetermined amount. Preferably, the increment corresponds to an increase of 1 cent in an amount of money represented by the count number.

The processor 10 includes a comparator means to

compare the count number with the stored random number generated as described above. The count number is also transmitted by processor 10 to display means formed by a display interface 15 and a dot matrix display 16. Display 16 represents the count number stored in the processor 10 in visual form and is updated each time that number is incremented by receipt of a signal from a poker machine (not illustrated).

Incrementing signals received from connected poker machines (not shown) by interface 11 are multiplexed into a lesser number of data lines and transmitted to the processor 10 with an address code. From the address code and date line number the processor 10 is able to identify and store the identity of the input of interface 11 that received a given incrementing signal thus providing means to record the identity of the poker machine that emitted the last incrementing signal if the random number and the counted number are equal. When the processor 10 determines that the count number is equal to the stored random number, the apparatus is placed in a hold mode by the processor 10 and the display 16 is operated via interface 15 to alternately represent the count number and an indication of the identity of the poker machine that emitted the last incrementing signal. Preferably, identification of the poker machine is by way of an alloted machine number.

The amount of money corresponding to the count number displayed is awarded to the person playing the

poker machine identified on the display as an additional prize. The amount of the prize is payed manually by authorised staff. After the awarding of a prize the apparatus is reset preferrably by operation of a key switch (not illustrated) connected with input 12. The count number can be preset to a minimum value to induce people to play connected poker machines.

The apparatus can also include decorative and attention attracting lighting (not shown). The operation of the lights is effected by means of the processor 10 and interface 11 in a substantially known manner.

Power to the apparatus is provided from mains supply via a low voltage transformer. The various components are each provided with appropriate regulators.

The apparatus will now be described in further detail with reference to the circuit diagrams of Figures 2, 3 and 4. Only those parts of each circuit necessary to understand the invention are described in detail.

Referring firstly to Figure 3, the processor circuit includes a 6802 P Central Processing Unit (CPU) 17, a 6116LP3 Random Access Memory (RAM) 18 and 2716 Programmable Read Only Memories (PROM) 19. A 6821 P Peripheral Interface Adaptor 20 is provided to interface with the circuit shown in Figure 3 via 50 plug 21. Power is provided to the circuit via a plug 22 and a 7805 Regulator 23.

A 74LS139 Multiplex Integrated Circuit 24 operates in conjunction with CPU 17 and associated operating

software to perform chip selection. A LM555 integrated circuit 25 acts as a circuit power monitor to provide RESET to CPU 17 on power up or power down. A CD 4020 binary counter 26 divides the clock pulse from CPU 17 to provide regular interrupt pulses at approximately 2 millisecond durations.

When external power is not available via plug 22 a standby voltage VB is provided to RAM 18 by a nickel - cadmium battery 27 which is connected to a charging circuit.

Output to the circuit of Figure 4 is provided by a 20 line connector plug 28. Connector plug 29 is provided for external communication to the CPU 17 and does not contribute to the invention.

Figure 3 is the circuit diagram of an interface from poker machines (not shown) to the processing circuit of Figure 2. For the purposes of a clarity only one poker machine coupling circuit 30 is shown and only two of three CD405 two multiplexing switches 31 are illustrated. The interface circuit provides for connection for up to 24 poker machines.

Input from each poker machine is electrically isolated by means of the coupling circuit 30 which includes a 4N35 opto-coupling device. Input pulses for the coupling circuit 30 are obtained from the solenoid of the connected poker machine stroke or turnover meter. Using a 4N35 opto-coupling device the power drawn from the poker machine is less than 3% of the normal stroke

meter power consumption. In practice it has been found that complete electrical isolation of each poker machine can be important to avoid errors and damage resulting from stray signals induced in the connecting lines.

The output from each opto-coupling circuit 30 is fed to an individual input (CH.5 in the illustrated arrangement) of multiplex switches 31. Three multiplex switches 31 are provided to give 24 individual input channels. The 24 input channels are multiplexed into 6 data lines D_0, D_1, D_2, D_3, D_4 D_5. The multiplexing is effected by a CD 4013 dual D-type flip-flop 32 which is driven by a clock pulse from a NE 555 astable oscillator 33. Flip-flop 32 provides an address to switches 31 so as to cyclically connect one of each group four inputs to the respective data line. An output from each stage flip-flop 32 provides one bit of a two-bit address which is supplied via an address line A_o, A_1, to the circuit of Figure 3.

Figure 4 is a circuit diagram of a display drive interface which drives a 5 X 7 dot matrix display (not shown). A 6821 interfacing integrated circuit 40 is provided to receive the output of circuit of Figure 2 via plug 41. The interface 40 drives six 4099 8-bit address latches 42. For sake of clarity only 3 of the address latches 42 are illustrated. Each latch 42 has a chip select $\overline{CS}$, a data input D and three address lines A_0, A_1, A_2. The upper most latch 42 shown in Figure 4 drives seven rows of the display and the remaining 5

meter power consumption. In practice it has been found that complete electrical isolation of each poker machine can be important to avoid errors and damage resulting from stray signals induced in the connecting lines.

The output from each opto-coupling circuit 30 is fed to an individual input (CH.5 in the illustrated arrangement) of multiplex switches 31. Three multiplex switches 31 are provided to give 24 individual input channels. The 24 input channels are multiplexed into 6 data lines D_0, D_1, D_2, D_3, D_4 D_5. The multiplexing is effected by a CD 4013 dual D-type flip-flop 32 which is driven by a clock pulse from a NE 555 astable oscillator 33. Flip-flop 32 provides an address to switches 31 so as to cyclically connect one of each group four inputs to the respective data line. An output from each stage flip-flop 32 provides one bit of a two-bit address which is supplied via an address line A_0, A_1, to the circuit of Figure 3.

Figure 4 is a circuit diagram of a display drive interface which drives a 5 X 7 dot matrix display (not shown). A 6821 interfacing integrated circuit 40 is provided to receive the output of circuit of Figure 2 via plug 41. The interface 40 drives six 4099 8-bit address latches 42. For sake of clarity only 3 of the address latches 42 are illustrated. Each latch 42 has a chip select $\overline{CS}$, a data input D and three address lines A_0, A_1, A_2. The upper most latch 42 shown in Figure 4 drives seven rows of the display and the remaining 5

latches 42 each drive five columns of the matrix. The latches 42 perform a standard mutilplex function to drive the display (not shown) and the latched outputs are amplified by a ULN 2003 Transistor Array 43. It will be apparent that because latches 42 only latch a single line of the dot matrix display at any one instant a continuity of processor operation is required for a full display. Accordingly, protection is provided against for an enormously large prize being awarded in the event of a processor malfunction. Moreover, because latches 42 are under control of CPU 17 which also controls the remainder of the apparatus, the display will not operate independently thus further safeguarding against erroneous prize awards.

In operation the main elements of the circuits shown in Figures 2, 3 and 4 operate as follows. The CPU 17 is driven by operating software in the known manner. Initial powering of the circuit results in a reset command from power monitor 25 to CPU 17 which initializes RAM 18 from PROM 19. If the apparatus has been operating previously and the RAM 18 and PROM 19 respond correctly to initialisation, CPU 17 initiates the process of selecting a random number. If RAM 18 and PROM 19 do not respond correctly CPU goes into a sleep mode until a system reset command is performed in response to an external control signal from switches (not shown) connected with the interface of Figure 2. After a system reset operation the CPU 17 also initiates the process of

selecting a random number.

The random number is gereated by the CPU 17 cyclically reading each one of a table of numbers stored in PROM 19 and storing into a location in RAM 18 the last number read. In this way the numbers in the table are cycled through the location in RAM 16 continuously until the counter is stopped. The numbers in the table are numbers in a selected range. The range can be adjusted in a substantially known manner by externally generated control signals transmitted to CPU 17. The numbers are randomly arranged in the table locations in PROM 19.

The random number is the number in the location in RAM 18 when the cycling is stopped. The CPU 17 will stop the cycling process either on detection of an external control pulse from the controls associated with the apparatus (not shown) or on detection of an incrementing signal from one of the connected poker machines (not shown). In either case an additional degree of randomness is introduced by the varying time that the counter will be allowed to cycle.

The remaining functions of the apparatus are performed by a cycle of operations controlled by CPU 17 and its operating software. The following operations are cyclically performed.

1. Detection of incrementing pulses. As described above interface of Figure 3 multiplexes incrementing pulses from twenty four poker machines into six data channels and two address channels. These channels are

continously scanned by CPU 17. On detection of a pulse from one of the poker machines, CPU 17 increments a first scratch pad in RAM 18 by one. At the same time the data line number and address number are decoded. The product of line number and address number form a machine identification number which is stored in a second scratch pad. This process is repeated at each detection of an incrementing pulse so that the first scratch pad records the number of pulses and the second scratch pad always contains the identification number of the poker machine that emitted the last incrementing pulse.

2. Incrementing Counter. In this operation CPU 17 first checks whether the number in the first scratch pad is zero. If it is zero no incrementing is required and the next operation is performed. If the number in the scratch pad is non-zero the CPU 17 deducts one from that value and provided a match flag (see infra) is not detected CPU 17 adds one to a counting location in RAM 18.

3. Matching. In each operation cycle CPU 17 compares the number in the counting location of RAM 18 with the random number separately stored in RAM 18. If the numbers are not equal the next operation is performed. If the numbers are equal CPU 17 generates a match flag. The match flag prevents further incrementing of the counting location and also changes the display read out as described below.

4. Display. In each cycle CPU 17 produces an output to the interface of Figure 4 so that the number in the

counting location of RAM 18 is represented on the dot matrix display. If a match flag is detected however, CPU 17 provides an output which results in the identification number in the second scratch pad being alternately represented on the display with the number in the counting location of RAM 18 to indicate that a prize is to be awarded to the player of that machine. That is, the machine which emitted the last incrementing signal if the count number and random number are equal.

After a prize has been awarded the apparatus is reset by operation of external controls referred to above and selection of a new random number is initiated.

The arrangement shown in Figures 2 to 4 also includes provision for generation of an audio signal to attract attention when a prize is to be awarded.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A random payment awarding apparatus for connection to a plurality of poker machines each adapted to produce an incrementing signal at each operation thereof, said apparatus comprising means to generate and store a random number within a selected range; counting means adapted to increment through the numbers in said range, each increment being effected on receipt of an incrementing signal from one of said poker machines; comparator means to compare said random number and the number held in said counting means; means to record the identity of the poker machine that emitted the last incrementing signal if said random number and the number held in said counting means are equal; and display means to display the number held in said counting means after each said increment and operable to display a prize award indication and the identity of the poker machine that emitted the last incrementing signal if said random number and the number held in said counting means are equal.

2. An apparatus as claimed in claim 1 wherein said random number is indicative of an amount of money to be payed to the player playing the machine which emitted the last incrementing signal.

3. An apparatus as claimed in claim 1 or claim 2 wherein each poker machine is electrically isolated from the random payment awarding apparatus.

4. An apparatus as claimed in claim 3 wherein each poker machine is electrically isolated by means of

opto-coupling device.

5. An apparatus as claimed in any one of claim 1 to 4 wherein the selected range is adjustable.

6. An apparatus as claimed in any one of claims 1 to 5 wherein said means for generating a random number comprises a free running counter which cyclically counts through the numbers in said selected range and the random number is selected by stopping the counter.

7. An apparatus as claimed in claim 6 wherein said selected range of numbers is stored in programmable read only memory and the cyclic counting is performed by a central processing unit sequentially reading the stored numbers.

8. An apparatus as claimed in any one of claims 1 to 6 wherein incrementing signals from the poker machines are multiplexed into a lesser number of data lines.

9. An apparatus as claimed in any one of claims 1 to 8 wherein said display means comprises a dot matrix display in which only the dots in a single line are latched on at any one time.

10. An apparatus as claimed in any one of claims 1 to 9 wherein a malfunction of the apparatus will prevent said display means from displaying a prize award indication.

11. An apparatus as claimed in any one of claims 1 to 9 wherein the incrementing signal is generated by the stroke meter of a poker machine.

12. A random payment awarding appartatus substantially as described with reference to the accompanying drawings.

DATED this 7th day of February, 1986

BORIS FRANKOVIC AND JOHN DOMENIC FAZZOLARE

Attorney: ROBERT G. SHELSTON

Fellow Institute of Patent Attorneys of Australia

of SHELSTON WATERS

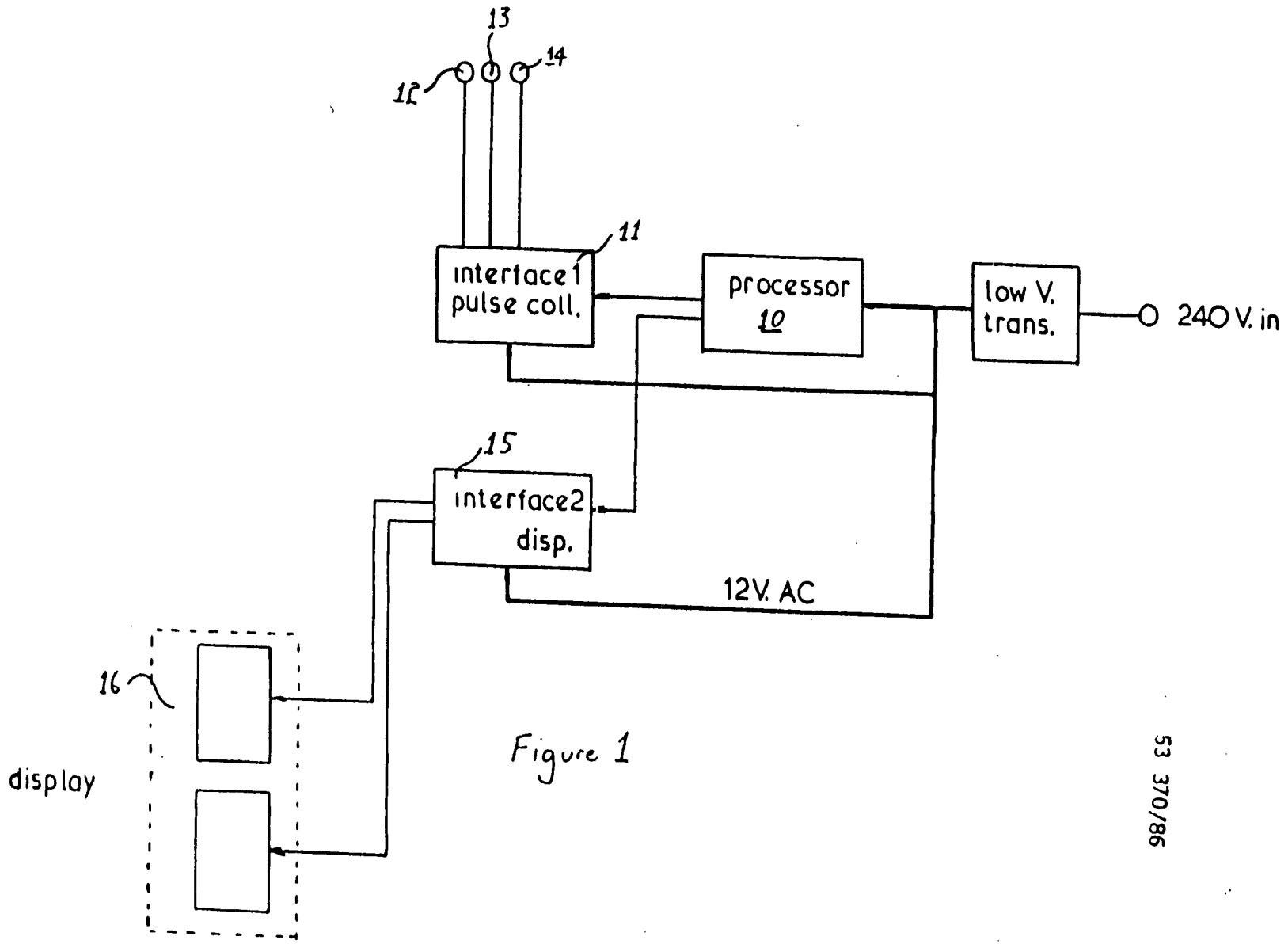

Figure 1

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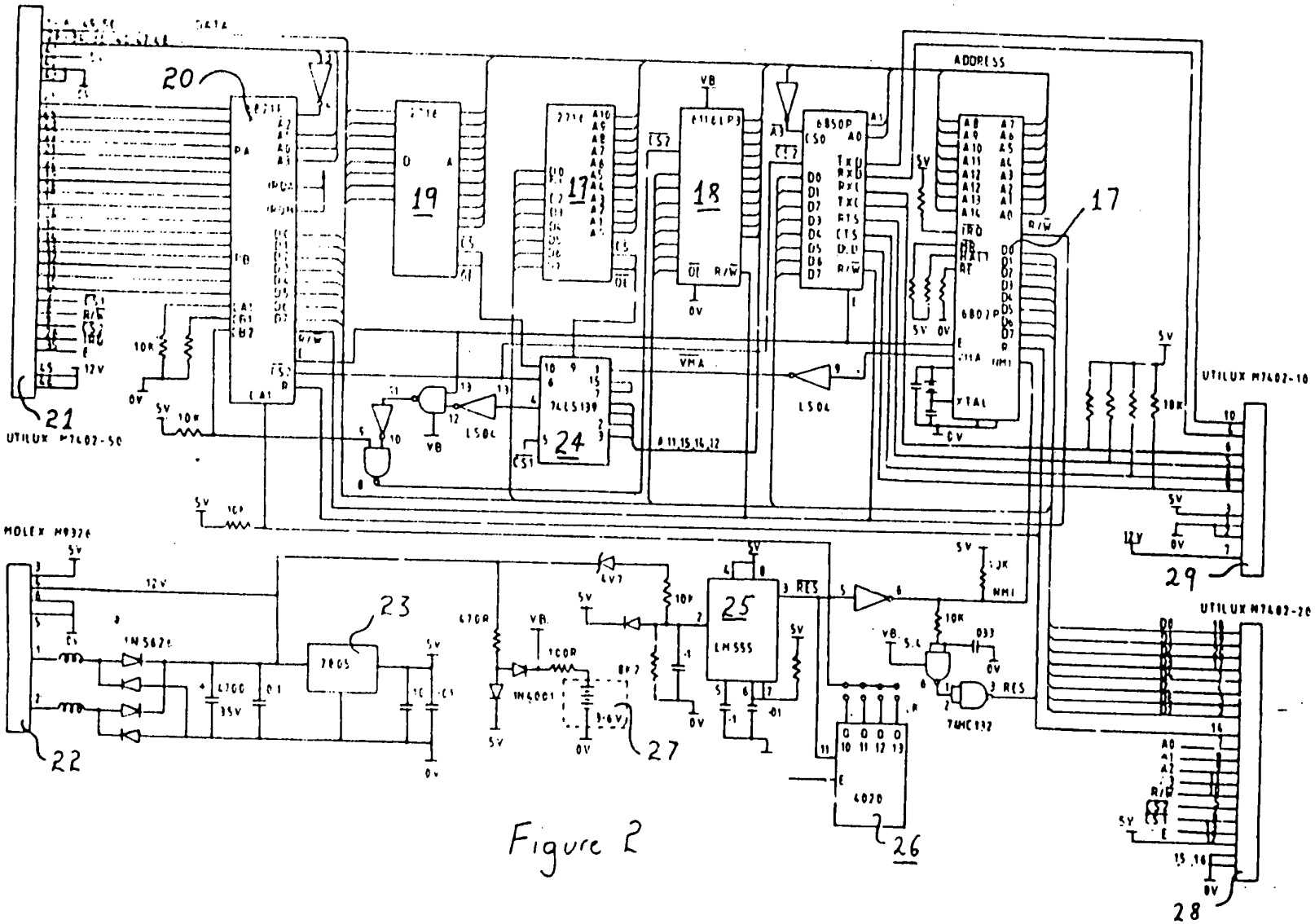
20
19
17
18
24
25
23
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21
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28
29
ADDRESS
DATA
UTILUX M7402-10
UTILUX M7402-20
UTILUX M7402-30
MOLEX M9326
74LS139
LS04
LM555
7805
4070
74HC132
1N5820
1N4001
6802P
6850P
6116LP3
VMA
R/W
RES
NMI
VB
5V
12V
0V

Figure 2

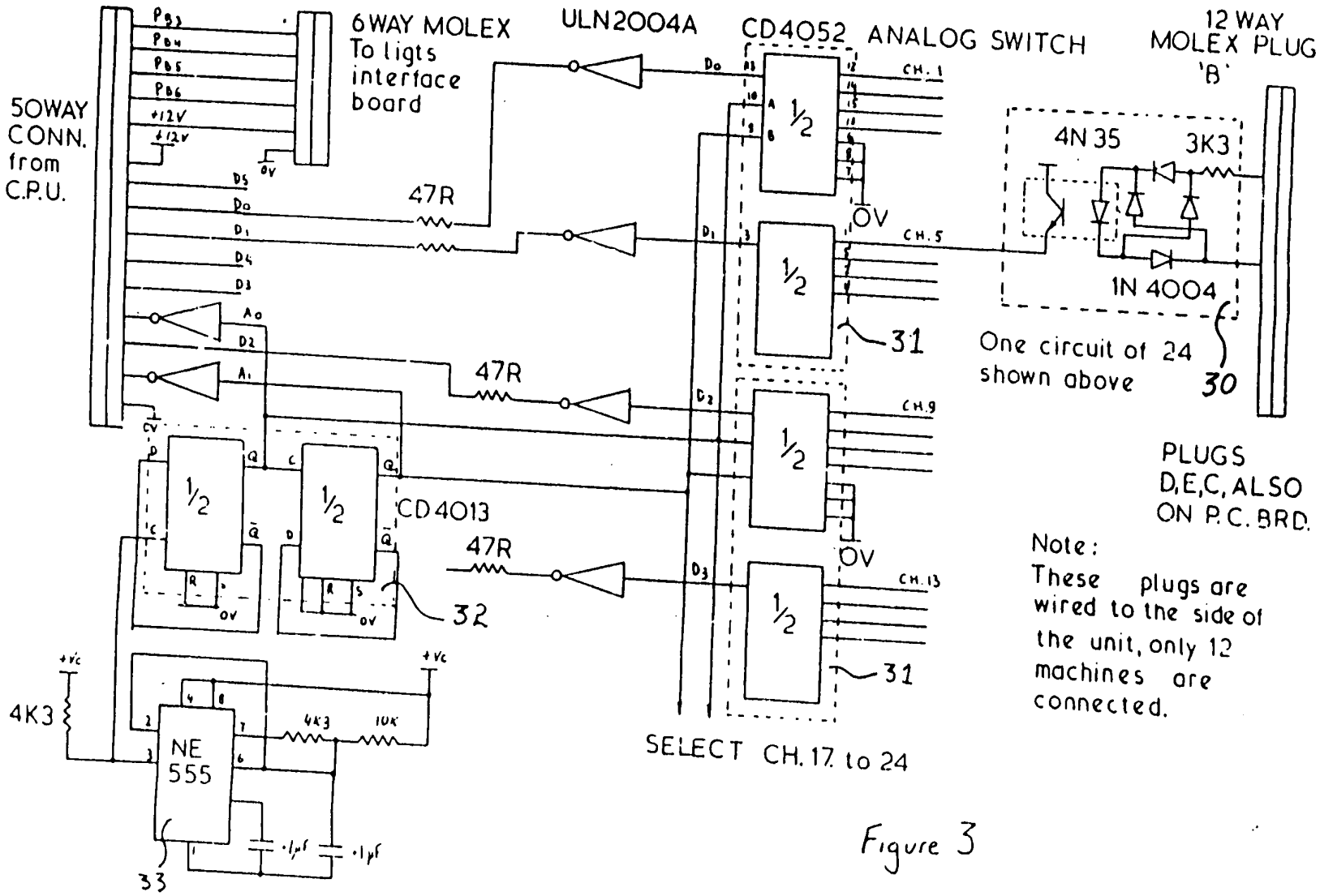
50WAY CONN. from C.P.U.
6WAY MOLEX To ligts interface board
ULN2004A
CD4052 ANALOG SWITCH
12 WAY MOLEX PLUG 'B'
47R
47R
47R
4N 35
3K3
1N 4004
One circuit of 24 shown above
30
31
31
32
33
CD4013
NE 555
4K3
10K
SELECT CH. 17 to 24
PLUGS D,E,C, ALSO ON P.C. BRD.
Note: These plugs are wired to the side of the unit, only 12 machines are connected.

Figure 3

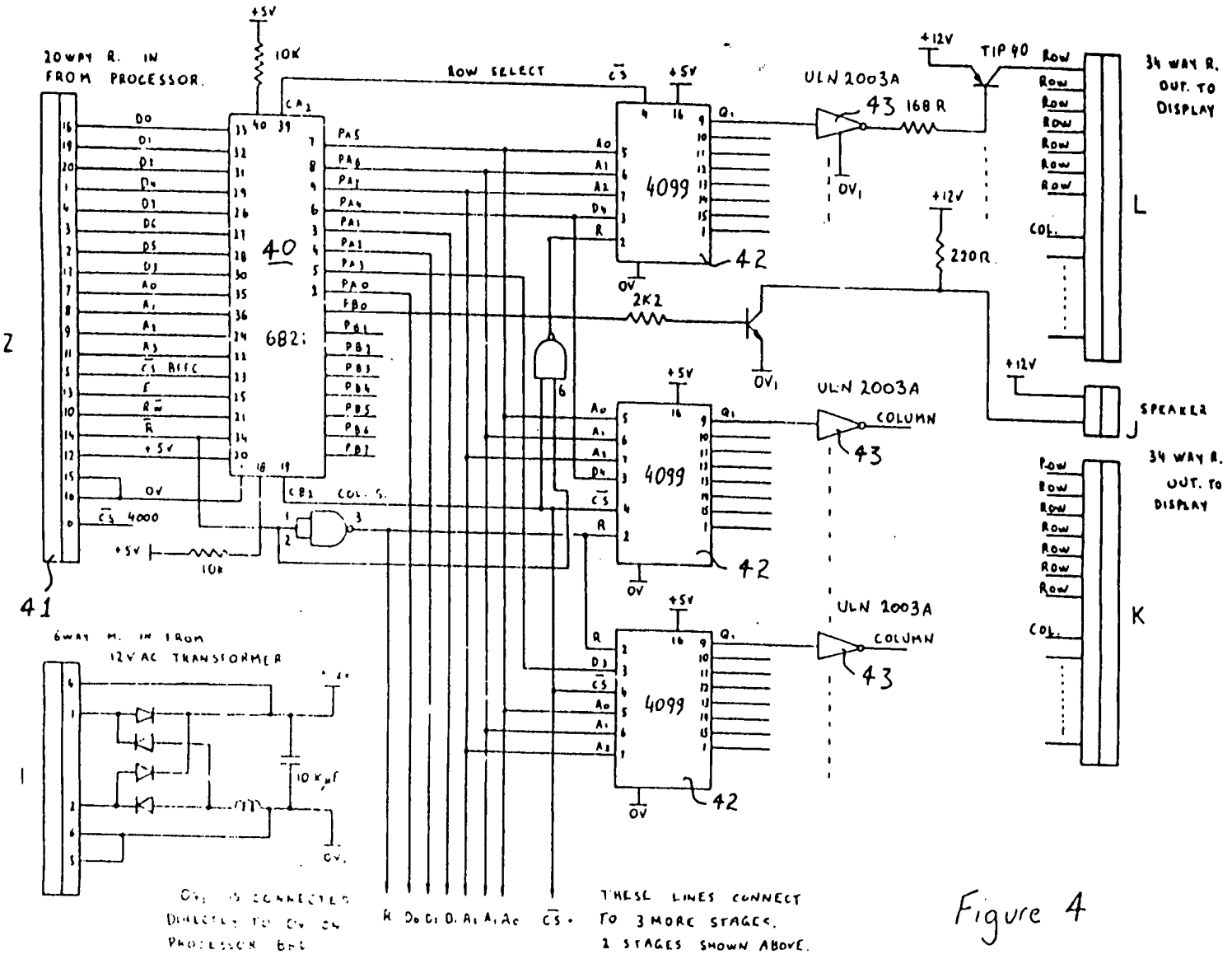

Figure 4